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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 42390.P7068 Total Pages 2

First Named Inventor or Application Identifier Peng Cheng

Express Mail Label No. EL034431764US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
   (Submit an original, and a duplicate for fee processing)
2. X Specification (Total Pages 18)
   (preferred arrangement set forth below)
   - Cover Sheet
   - Descriptive Title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claims
   - Abstract of the Disclosure
3. X Drawings(s) (35 USC 113) (Total Sheets 3)
4. X Oath or Declaration/Power of Attorney (Total Pages 4)
   a. x Unsigned
   b. ___ Copy from a Prior Application (37 CFR 1.63(d))
   (for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**
   i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. ___ Incorporation By Reference (useable if Box 4b is checked)
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ___ Microfiche Computer Program (Appendix)
7. ___ Nucleotide and/or Amino Acid Sequence Submission
   (if applicable, all necessary)
   a. ___ Computer Readable Copy
   b. ___ Paper Copy (identical to computer copy)
   c. ___ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
10. _____ English Translation Document (if applicable)
11. _____ a. Information Disclosure Statement (IDS)/PTO-1449
_____ b. Copies of IDS Citations
12. _____ Preliminary Amendment
13. _X_ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)
b. Statement filed in prior application, Status still proper and desired
15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. _X_ Other: Certificate of Mailing (1 page in duplicate)

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:

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of prior application No: _

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P7068 PATENT

TRANSISTOR STRUCTURE HAVING SILICIDE SOURCE/DRAIN EXTENSIONS AND METHOD FOR MAKING SAME

Inventors: Peng Cheng
Brian S. Doyle
Gang Bai

"Express Mail" mailing label number EL034431764US

TRANSISTOR STRUCTURE HAVING SILICIDE SOURE/DRAIN EXTENSIONS AND METHOD FOR MAKING SAME

Inventors: Peng Cheng
Brian S. Doyle
Gang Bai

Background of the Invention

Field of the Invention

The invention relates to the field of semiconductor integrated circuits, and more particularly relates to metal-oxide-semiconductor (MOS) field effect transistors (FETs).

Background

For many years integrated circuits incorporating metal-oxide-semiconductor field effect transistors (MOSFETs) have been manufactured with materials such as doped polycrystalline silicon to form the gate electrode, and doped crystalline silicon to form the source/drain terminals. Significant effort has been devoted to scaling down the physical dimensions of MOSFETs in order to increase the functionality of integrated circuits by including more transistors on each integrated circuit.

As devices were scaled down in size, there was a corresponding increase in the resistances associated with the source/drain terminals. Typically, as the linear dimensions of transistors were reduced, the depth of the source/drain terminals was reduced. The thickness of the source/drain terminals, i.e., junction depth, was reduced, as required for maintaining appropriate electrical characteristics in the scaled down MOSFETs. With thickness, that is, the junction depth, of the source/drain terminals reduced, the cross-sectional area of the source/drain terminals was reduced, which resulted in greater electrical resistance to signals propagating through the source/drain terminals.

What is needed are structures that provide low sheet resistivities for MOSFET source/drain terminals, and methods for making the same.

Summary of the Invention

Briefly, a MOSFET includes a double silicided source/drain structure wherein the source/drain terminals include a silicided source/drain extension, a deep silicided source/drain region, and a doped semiconductor portion that surrounds a portion of the source/drain structure such that the silicides are isolated from the MOSFET body node.

In a further aspect of the present invention, a barrier layer is formed around a gate electrode to prevent electrical shorts between a silicided source/drain extension and the gate electrode. A deep source/drain is then formed, self-aligned to sidewall spacers that are formed subsequent to the silicidation of the source/drain extension.

Brief Description of the Drawings

Fig. 1 is a schematic cross-sectional view of a conventional FET having sidewall spacers and a silicide layer overlying the source/drain terminals, and gate electrode.

Fig. 2 is a schematic cross-sectional view of a partially fabricated FET having a patterned polysilicon gate electrode disposed over a gate dielectric layer, the gate electrode having a silicon nitride barrier layer disposed thereon.

Fig. 3 is a schematic cross-sectional view of the FET of Fig. 2, wherein doped source/drain extensions have been formed in a self-aligned manner adjacent to the gate electrode.

Fig. 4 is a schematic cross-sectional view of the FET of Fig. 3 after the source/drain extensions have been silicided.

Fig. 5 is a schematic cross-sectional view of the FET of Fig. 4, after the top portion of the silicon nitride barrier has been removed and sidewall spacers have been formed.

Fig. 6 is a schematic cross-sectional view of the structure of Fig. 5, after a deep source/drain junction, disposed beneath the silicided source/drain extensions, has been formed.

Fig. 7 is a schematic cross-sectional view of the structure of Fig. 6, after the polysilicon gate electrode has been silicided and a deep source/drain silicide layer has been formed.

Detailed Description

Overview

Embodiments of the present invention provide an MOS transistor structure having silicided source/drain extensions. In contradistinction to conventional MOS transistor structures in which the source/drain extension is heavily doped, the silicided source/drain extension in embodiments of the present invention provide substantially reduced sheet resistance in the source/drain extension regions. The reduced resistance of the silicided source/drain extension in embodiments of the present invention makes it possible to significantly reduce the doping concentration in the source/drain extension region thereby reducing the lateral out-diffusion that conventionally occurs during the dopant activation process.

Terminology

The terms, chip, integrated circuit, monolithic device, semiconductor device, and microelectronic device, are often used interchangeably in this field. The present invention is applicable to all the above as they are generally understood in the field.

The term "gate" is context sensitive and can be used in two ways when describing integrated circuits. Gate refers to a circuit for realizing an arbitrary logical function when used in the context of a logic gate. However, as used herein, gate refers to the insulated gate terminal of a three terminal FET when used in the context of transistor circuit configurations or formation of transistor structures. The expression "gate terminal" is generally interchangeable with the

expression "gate electrode". A FET can be viewed as a four terminal device when the semiconductor body is considered, for the purpose of describing illustrative embodiments of the present invention, the FET will be described using the traditional gate-drain-source, three terminal model.

Channel, as used herein, refers to that portion of the semiconductor body that underlies the gate dielectric, is bounded by the source/drain terminals, and is the region of the FET where current flows between the source and drain terminals.

Polycrystalline silicon is a nonporous form of silicon made up of randomly oriented crystallites or domains. Polycrystalline silicon is often formed by chemical vapor deposition from a silicon source gas or other methods and has a structure that contains large-angle grain boundaries, twin boundaries, or both. Polycrystalline silicon is often referred to in this field as polysilicon, or sometimes more simply as poly.

Source/drain terminals refer to the terminals of a FET, between which conduction occurs under the influence of an electric field, subsequent to the inversion of the semiconductor surface under the influence of a vertical electric field resulting from a voltage applied to the gate terminal. Generally, the source and drain terminals are fabricated such that they are geometrically symmetrical. With geometrically symmetrical source and drain terminals it is common to simply refer to these terminals as source/drain terminals, and this nomenclature is used herein. Designers often designate a particular source/drain terminal to be a "source" or a "drain" on the basis of the voltage to be applied to that terminal when the FET is operated in a circuit. Typically, source/drain terminals are doped with either donor (n-type) or acceptor (p-type) atoms to create the desired electrical characteristics.

The terms wafer and substrate are generally used interchangeably in this field and are so used herein. A reference to a wafer or substrate may include a bare or pure semiconductor substrate, with or without doping, a semiconductor substrate incorporating one or more device layers at any stage of processing,

other types of substrates incorporating one or more semiconductor layers, substrates having silicon on insulator (SOI), GaAs substrates, sapphire substrates, or any other substrate suitable for processing microelectronic or microelectromechanical devices.

One result of scaling down the dimensions of FETs has been an increase in, the sheet resistivities associated with the source/drain terminals. An approach commonly used to decrease the sheet resistivities of the scaled down source/drain terminals, has been to form a layer having a relatively low sheet resistivity, in parallel with the source/drain terminals. For example, various refractory metal silicides (e.g., titanium silicide) were formed over the surfaces of the source/drain terminals. In this way, the effective sheet resistivity of the source/drain terminals was reduced.

Fig. 1 illustrates a conventional FET structure having a silicided gate electrode and silicided source/drain terminals. More particularly, a FET **10** is formed between shallow trench isolation structures **12**, which define an active region of the substrate **14**. A gate electrode comprising a polysilicon portion **16**, and a silicide portion **18** are formed over active region of the substrate **14** with a gate dielectric layer **20** disposed therebetween. Source/drain terminals, disposed in active region of the substrate **14** are disposed adjacent to the gate electrode, and include doped regions **22**, and silicided regions **24**. Silicide regions **24** have lower sheet resistivities as compared to doped regions **22**. Physically forming silicide regions **24** superjacent doped regions **22** results in silicide region **24** being electrically in parallel with doped region **22**. In this way the effective electrical resistance of the source/drain terminals is conventionally reduced compared to the resistance of the doped regions alone.

However, as FET dimensions scale down into the deep submicron region, silicidation of the source/drain terminals is not adequate to compensate for the high resistivity of the shallow source/drain extensions. One approach to reducing the limitation on transistor performance that high source/drain resistivity imposes, is to increase the doping concentration in the source/drain extensions.

Unfortunately, the high doping concentration of these source/drain extensions results in out-diffusion of dopants into the channel portion of the FET, which in turn degrades the electrical performance of the transistor. Such adverse effects include undesired changes in threshold voltage, and decreased mobility due to higher scattering in the channel portion.

Embodiments of the present invention, provide FET structures with relatively low resistivity source/drain extensions, while not requiring a high doping concentration to achieve such low resistivities. More particularly, embodiments of the present invention provide FETs with metal silicide source/drain extensions. These metal silicide source/drain extensions have significantly reduced the sheet resistance in the source/drain extension region. In view of the reduced sheet resistance, the doping concentration in the source/drain extension region can be reduced, which in turn, results in reduced out-diffusion in to the channel region.

In the following description, numerous specific details are set forth such as specific materials, patterns, dimensions, etc., in order to provide a thorough understanding of the present invention. In other instances, well known materials or methods haven not been described in detail in order to avoid obscuring the invention.

An illustrative structure and process, each embodying the present invention are described in conjunction with Figs. 2-7. Conventional semiconductor processing steps may be used up through the formation of patterned polysilicon disposed over a gate dielectric layer, which in turn is disposed upon a substrate. Those skilled in the art will appreciate that drawing figures are for illustration purposes and each layer shown may not be shown to scale with respect to the other layers. For example, in actual devices the substrate is much, much thicker than is shown relative the gate dielectric layer. Nonetheless those skilled in the art will readily understand the structures and process operations described in conjunction with the schematic cross-sections of Figs. 2-7. Referring now to Fig. 2, a silicon substrate **102** has formed thereon on dielectric layer **104**. Typically dielectric layer **104** may be an oxide of silicon,

however the present invention is not limited to any particular material or combination of materials. For example, the present invention may be used in conjunction with dielectrics that are formed from materials such as, but not limited to, nitrides, metal oxides, rare earth oxides, or any combination thereof. As indicated in Fig. 2, a polysilicon layer is patterned to form a gate electrode **106**. The deposition and patterning of polysilicon is very well known in this field. Although polysilicon is typically used to form gate electrode **106**, other materials may used to form a gate electrode, and the present invention is not limited to any particular material or combination of materials to form gate electrode **106**. Gate electrode **106** has a barrier layer **108** formed thereon such that the material that makes up gate electrode **106** is covered on all its sides. As shown in the schematic cross-section of Fig. 2, a top surface, and sidewall surfaces of gate electrode **106** are covered by barrier layer **108**, and a bottom surface of gate electrode **106** is in contact with dielectric layer **104**.

Still referring to Fig. 2, in the illustrative embodiment of the present invention, dielectric layer **104** is an oxide of silicon, gate electrode **106** is polysilicon, and barrier layer **108** is a silicon nitride layer. Nitride barrier layer **108** is formed by nitridizing polysilicon gate electrode **106**. Typically, the nitride layer is very thin, for example, approximately 10 angstroms, so that it will not significantly affect the source/drain extension length. At the same time, the nitride layer should be thick enough to prevent an electrical short between a yet to be formed silicide source/drain extension structure, and the gate electrode.

Referring now to Fig. 3, it can be seen that a portion of dielectric layer **104** has been removed. Conventional etch techniques can be used to remove dielectric **104** where it is not covered by gate electrode **106** or barrier layer **108**. Those skilled in the art will recognize that an etchant should preferentially remove dielectric **104** as compared to barrier layer **108**. In this illustrative embodiment of the present invention, a ion implantation operation is performed after the dielectric layer removal operation. Ion implantation is a well known method in which impurities, sometimes referred to as dopants, are introduced

into various layers of a microelectronic device in order to modify their electrical properties. The implanted dopants may be p-type or n-type depending respectively on whether a p-channel or n-channel MOSFET is being fabricated. In this instance, the ion implantation operation forms source/drain extensions **110**, and is typically a shallow implant similar to those used in conventional CMOS (Complementary Metal Oxide Semiconductor) processes, however, the resulting doping concentration can be substantially less than that found in conventional source/drain extensions. In the illustrative embodiment of the present invention the doping concentration may be up to an order of magnitude lower. Those skilled in the art and having the benefit of the present disclosure will recognize that for any given implementation of the present invention, the doping concentration chosen is dependent on a number of design parameters including, but not limited to, the starting doping concentration in the substrate, the depth of the source/drain extension implant, the thermal budget for the complete process, and the nominal channel length of the MOSFET being fabricated.

Subsequent to the formation of source/drain extensions **110** by ion implantation, a dopant activation operation is performed. Dopant activation is well known in this field and typically involves heating at least portions of the substrate. During this high temperature dopant activation operation, some lateral out-diffusion from the source/drain extension into the channel region typically occurs. In embodiments of the present invention however, the amount of out-diffusion is smaller than in conventional processes because the doping concentration in the source/drain extension is substantially less. In one embodiment of the present invention, as shown in Fig. 3, the final depth of source/drain extension **110** is typically between 300 and 500 angstroms.

Subsequent to the formation of source/drain extension **110**, a first metal layer is deposited over substrate **102**, such that substrate **102** as well as barrier layer **108** are covered. The first metal is typically a metal that forms a silicide when reacted with silicon. Titanium and cobalt are examples of such metals. It is preferable to use a metal which will form a silicide that is stable during a

subsequent high temperature dopant activation operation. Such a dopant operation is typically performed at approximately 1000°C. Referring now to Fig. 4, the first metal layer is reacted with the exposed surface of the doped silicon regions that comprise source/drain extension **110** to form a silicide **112**. As shown in Fig. 4, silicide **112** forms over source/drain extension regions **110**. Reaction conditions that may be used to produce silicide **112** include rapid thermal processing at temperatures in the range of approximately 500°C-800°C for durations of approximately 20 seconds to 5 minutes. Barrier layer **108**, a thin nitride layer in the illustrative embodiment, prevents the silicidation of polysilicon gate electrode **106** such that an electrical short between gate electrode **106** and source/drain extension **110** does not occur. The depth of silicide **112** should be less than the depth of source/drain extension **110**. The lateral encroachment of silicide **112** into the channel region should be less than the length of the lateral out-diffusion of the dopants from source/drain extension **110**. In other words, silicide **112** should be surrounded, in the substrate, by the doped silicon source/drain extension **110**.

After silicide **112** is formed, unreacted portions of the first metal layer (not shown) are removed, typically by wet chemical etching. Removal of unreacted metal is well known in this field.

Referring now to Fig. 5, sidewall spacers **114** are formed adjacent to barrier layer **108**. Methods and materials for forming sidewall spacers are known in this field. The present invention is not limited to any particular method or materials for the formation of sidewall spacers **114**. Typically, a layer of material such as silicon nitride, silicon dioxide, or a combination thereof, is deposited on the substrate; and this layer is then anisotropically etched so that portions of the layer remain adjacent to the transistor gate structure. As is further shown in Fig. 5, that portion of barrier layer **108** which is exposed after the formation sidewall spacers **114** is removed, thereby exposing a top portion of polysilicon **106**.

In an alternative embodiment, barrier layer **108** may be removed prior to the formation of sidewall spacers **114** as long as the removal process does not adversely impact the characteristics of the transistor.

Referring now to Fig. 6, source/drains **116** are formed which are self-aligned to spacers **114**. Source/drains **116** are typically formed by ion implantation. Typically, n-type source/drains are formed by the implantation, and subsequent thermal activation, of arsenic or phosphorus ions. Similarly, p-type source/drains are typically formed by the implantation and subsequent thermal activation of boron ions. In this illustrative embodiment of the present invention, source/drain ion implantation is performed through silicide **112**. An implant such as this may typically have a dose $4x10^{15}$ atoms per cm^2 at an energy in the range of 1-50keV depending on the implanted species. Furthermore, silicide **112** must be stable during the thermal activation of the source/drain dopants. The thermal activation of the source/drain dopants typically takes place at approximately 1000°C. $CoSi_2$ and $TiSi_2$ are examples of silicides that meet the required constraints.

After the activation of the source/drain dopants, a second layer of metal is deposited over the surface of the substrate. The second layer of metal may be same as, or different from the first layer of metal. The second metal is reacted with the substrate so as to form a deep silicided region **120** within source/drains **116**. At substantially the same time as deep silicided region **120** is formed, polysilicon gate electrodes **106** are also silicided. It is preferable that the metal selected for use in this second silicidation reaction does not agglomerate on top of very narrow polysilicon lines. Nickel is a metal which meets this requirement and may be used to form a nickel silicide over the gate electrodes and source/drain regions.

The unreacted portions of the second metal are typically removed by a wet chemical etch. For example, a solution of $NH_4OH:H_2O_2:H_2O$ may be used to etch excess Ti.

Subsequent to removal of the unreacted portions of the second metal, conventional processing operations may be used to complete an integrated circuit including a MOSFET in accordance with the present invention.

Many variations of the processes and materials described above may be used to achieve similar end results. One alternative process may eliminate the operation in which the source/drain extension dopants are activated prior to the first silicidation operation. By eliminating this first activation operation, it is possible to achieve a sharper lateral dopant profile.

In another alternative embodiment, barrier layer **108** may be formed by a method other than the nitridation of a polysilicon gate electrode. For example, an extremely thin dielectric layer, such as approximately 10 angstroms of silicon nitride, may be deposited and an anisotropic etch operation then performed so as to form a spacer on the sides of the gate electrode. The spacer must be thick enough to prevent an electrical short between the silicided source/drain extension, and the gate electrode. The spacer must also be thin such that it does not substantially affect the length of the source/drain extension.

No limitation on the exact geometries of the various constituent parts of MOSFETs in accordance with the present invention are intended by the descriptions of illustrative embodiments herein.

Conclusion

Shallow source/drain extensions are used in scaled down MOSFETs in order to reduce the short channel effects that would otherwise occur. Conventionally, these source/drain extensions are formed from heavily doped silicon. The high level of doping in the source/drain extension is needed to reduce the sheet resistance of these structures. However, the high doping density results in significant out-diffusion during the dopant activation process. This out-diffusion adversely affects electrical performance of the MOSFET.

MOSFETs in accordance with the present invention include a silicide source/drain extension structure. A silicide source/drain extension structure can

provide reduced sheet resistance as compared to conventional heavily doped Si source/drain extensions. Consequently, the silicide source/drain extension structure does not require a high doping concentration. Since a lower doping concentration can be used in the silicide source/drain extension structure in accordance with the present invention, the adverse impact of lateral out-diffusion is reduced. In turn, the reduced lateral out-diffusion provides a transistor structure that requires less overlap between the source/drain extension and the gate electrode. A benefit of the present invention is that a more scalable transistor structure is achieved.

It will be understood by those skilled in the art that many design choices are possible within the scope of the present invention. For example, metals such as Ti or Ni may be used, but in order to use Ti or Ni, a disposable spacer process should be used to avoid high temperature activation. Additionally, the present invention is not limited to silicon substrates.

It will be understood that various other changes in the details, materials, and arrangements of the parts and steps which have been described and illustrated may be made by those skilled in the art without departing from the principles and scope of the invention as expressed in the subjoined Claims.

What is claimed is:

1. A method of forming a transistor, comprising:

forming a silicidation barrier on a patterned polysilicon layer;

implanting dopants to form a source/drain extension layer self-aligned to the patterned polysilicon;

forming a first silicide layer over the source/drain extension layer;

forming sidewall spacers adjacent to the patterned polysilicon;

removing a portion of the silicidation barrier from a top surface of the patterned polysilicon;

forming a second silicide layer self-aligned to the sidewall spacers; and

forming a third silicide layer on a top surface of the patterned polysilicon.

2. The method of Claim 1, wherein the second silicide layer and the third silicide layer are formed concurrently.

3. The method of Claim 1, wherein forming a silicidation barrier comprises nitridizing the patterned polysilicon layer.

4. The method of Claim 1, wherein forming the silicidation barrier comprises forming a silicon nitride layer on a top surface of the patterned polysilicon, and on at least one sidewall of the patterned polysilicon.

5. The method of Claim 1, wherein the silicidation barrier has a thickness sufficient to prevent silicidation of the polysilicon.

6. The method of Claim 1, further comprising depositing a layer of metal over the source/drain extension layer, wherein the metal is selected from the group consisting of titanium and cobalt.

7. The method of Claim 6, wherein further comprising depositing a layer of metal over the first silicide layer, wherein the metal is selected from the group consisting of nickel and cobalt.

8. The method of Claim 1, wherein the second and third silicide layers comprise nickel silicide.

9. The method of Claim 1, further comprising implanting dopants through the first silicide layer to form source/drains self-aligned to the sidewall spacers.

10. A method of forming a microelectronic device, comprising:

forming a patterned polysilicon layer over a dielectric layer, the dielectric layer disposed on a substrate, the patterned polysilicon having sidewalls and a top surface;

nitridizing the sidewalls and top surface of the polysilicon;

implanting first dopants into the substrate to form a source/drain extension layer;

forming a first silicide layer over the source/drain extension layer;

forming sidewall spacers adjacent to the sidewalls;

implanting second dopants through the first silicide layer into a source/drain region; and

forming a second silicide self-aligned to the sidewall spacers.

11. The method of Claim 10, further comprising thermally activating the first dopants prior to implanting the second dopant atoms.

12. The method of Claim 10 wherein the first and second silicides comprise different metals.

13. The method of Claim 10 wherein the first and second silicides comprise the same metal.

14. The method of Claim 10 wherein nitridizing the polysilicon produces a silicon nitride layer approximately 10 angstroms thick.

15. The method of Claim 10, further comprising forming an agglomeration-free silicide layer over the patterned polysilicon.

16. The method of Claim 10, further comprising removing the nitridized portion of the top surface of the gate electrode.

17. The method of Claim 10, wherein the second silicide layer is formed through the first silicide layer.

18. A microelectronic structure, comprising:

a gate electrode having sidewalls;

a silicidation barrier adjacent to the sidewalls;

a first silicide layer superjacent the gate electrode; and

a pair of source/drain terminals self-aligned to the gate electrode;

wherein the source/drain terminals comprise a first implanted region, a second silicide layer; a second implanted regions and a third silicide layer.

19. The microelectronic structure of Claim 18, wherein the second silicide layer is contained within the first implanted region.

20. The microelectronic structure of Claim 18, wherein the third silicide layer is thicker than the first implanted region.

ABSTRACT OF THE DISCLOSURE

A MOSFET includes a double silicided source/drain structure wherein the source/drain terminals include a silicided source/drain extension, a deep silicided source/drain region, and a doped semiconductor portion that surrounds a portion of the source/drain structure such that the silicides are isolated from the MOSFET body node. In a further aspect of the present invention, a barrier layer is formed around a gate electrode to prevent electrical shorts between a silicided source/drain extension and the gate electrode. A deep source/drain is then formed, self-aligned to sidewall spacers that are formed subsequent to the silicidation of the source/drain extension.

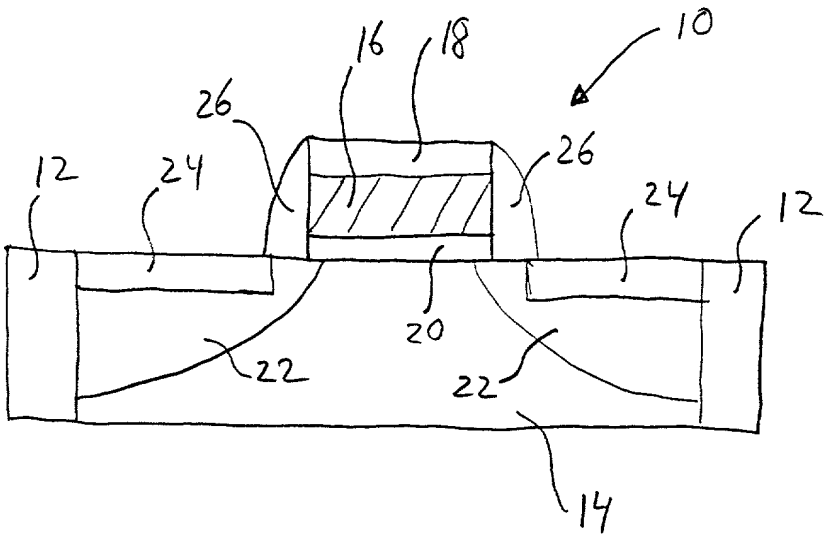

Fig. 1

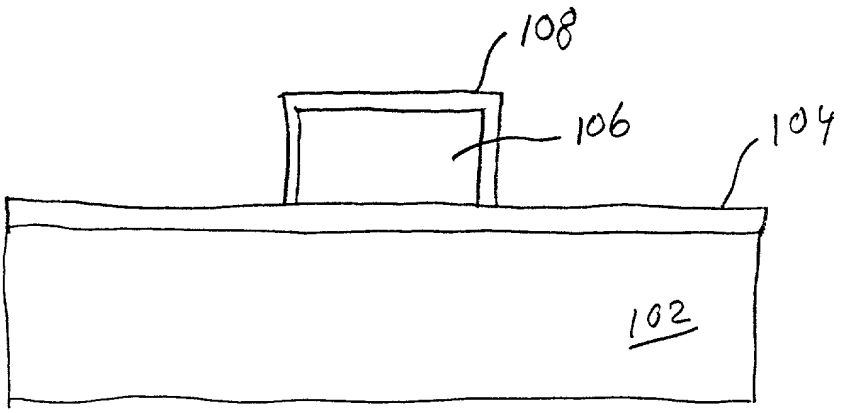

Fig. 2

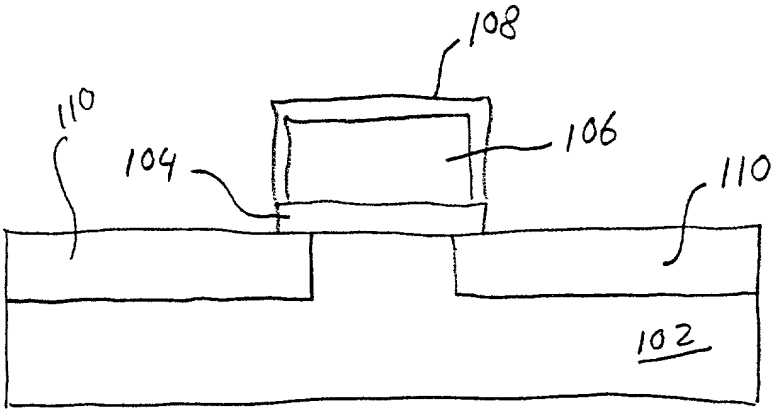

Fig. 3

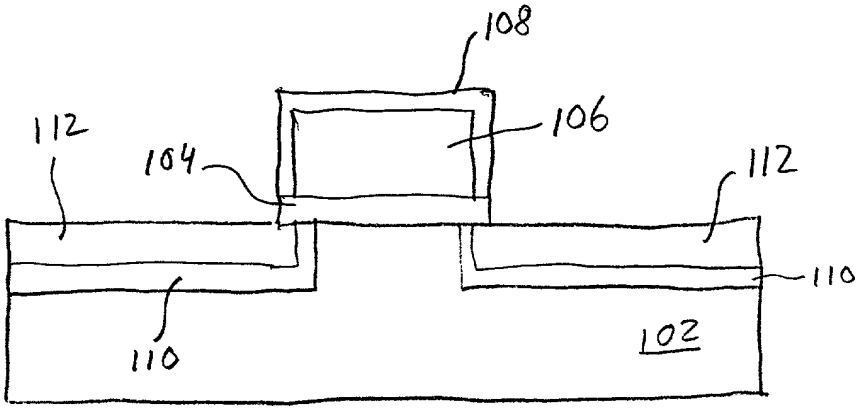

Fig. 4

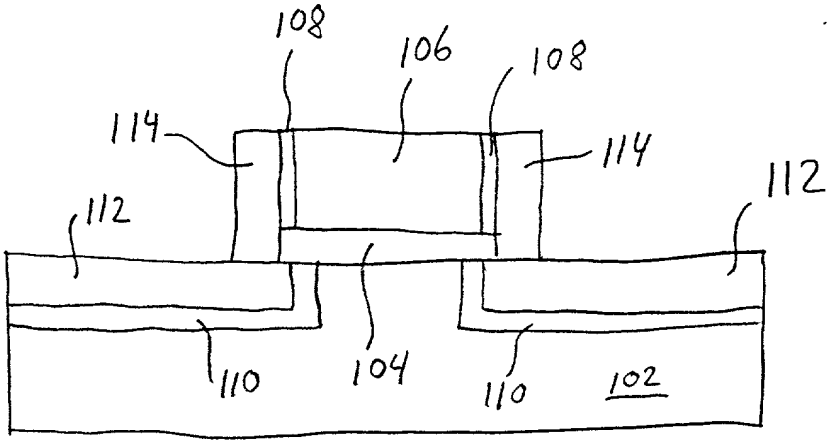

Fig. 5

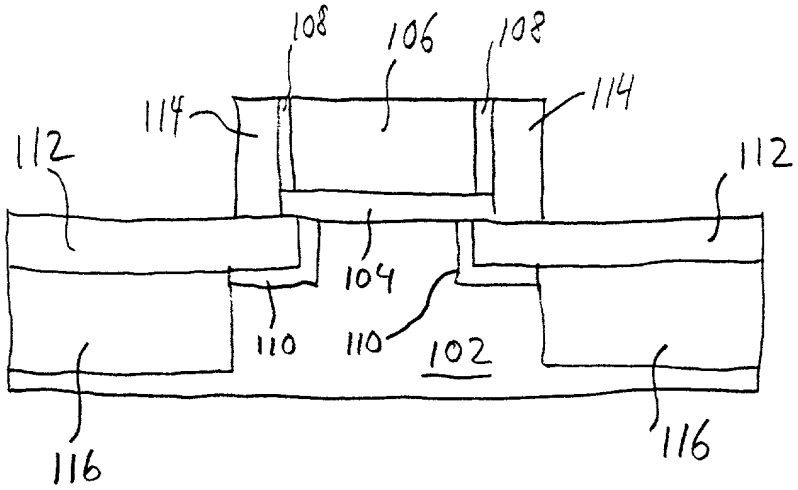

Fig. 6

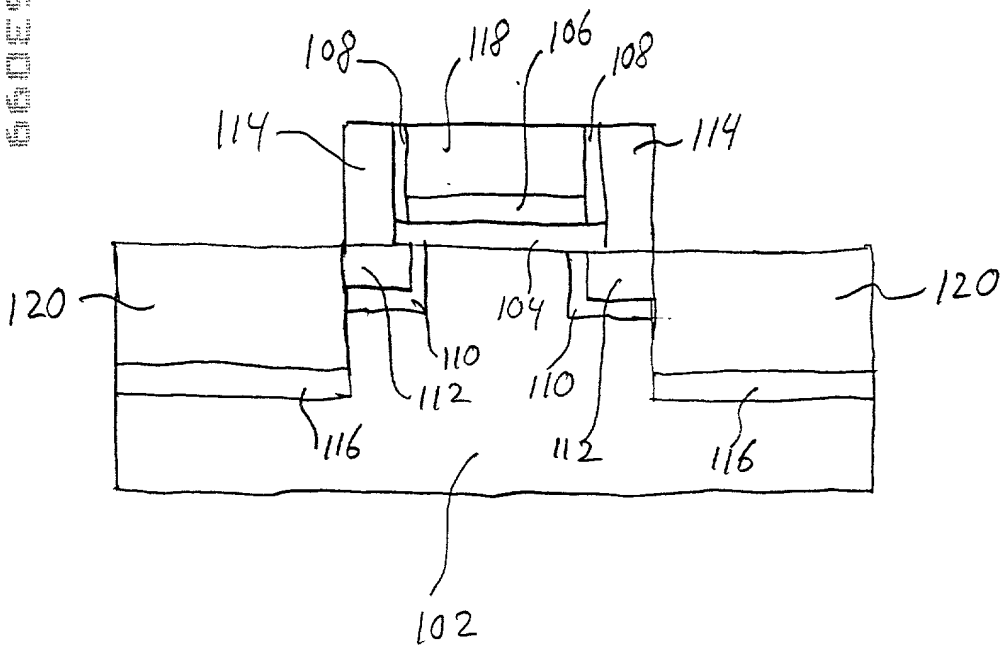

Fig. 7

Attorney's Docket No.: 42390.P7068 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

TRANSISTOR STRUCTURE HAVING SILICIDE SOURCE/DRAIN EXTENSIONS AND METHOD FOR MAKING SAME

the specification of which

_XX_ is attached hereto.
____ was filed on _____ as
United States Application Number _____
or PCT International Application Number_____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

I hereby appoint Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; Amy M. Armstrong, Reg. No. 42,265; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Yong S. Choi, Reg. No. P43,324; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; Barbara Bokanov Courtney, Reg. No. 42,442; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; Richard Leon Gregory, Jr., Reg. No. 42,607; Dinu Gruia, Reg. No. P42,996; David R. Halvorson, Reg. No. 33,395; Thomas A. Hassing, Reg. No. 36,159; Phuong-Quan Hoang, Reg. No. 41,839; Willmore F. Holbrow III, Reg. No. P41,845; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. 42,004; Thinh V. Nguyen, Reg. No. 42,034; Kimberley G. Nobles, Reg. No. 38,255; Babak Redjaian, Reg. No. 42,096; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Anand Sethuraman, Reg. No. P43,351; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; George G. C. Tseng, Reg. No. 41,355; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Stephen Warhola, Reg. No. 43,237; Charles T. J. Weigell, Steven D. Yates, Reg. No. 42,242; Reg. No. 43,398; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys, and James A. Henry, Reg. No. 41,064; Daniel E. Ovanezian, Reg. No. 41,236; Glenn E. Von Tersch, Reg. No. 41,364; and Chad R. Walsh, Reg. No. 43,235; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Cynthia Thomas Faatz, Reg No. 39,973; Sean Fitzgerald, Reg. No. 32,027; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Jeffrey S. Draeger, Reg. No. 41,000; Thomas Raleigh Lane, Reg. No. 42,781; Calvin E. Wells, Reg. No. P43,256; and Alexander Ulysses Witkowski, Reg. No. P43,280; my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Raymond J. Werner, Intel BLAKELY, SOKOLOFF, TAYLOR
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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